



FlashDiskModule 601 & 601PRO

40pin Vertical

Specification

Ver1.2

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Introduction

This IDE Flash Disk is a flash technology based with ATA interface flash memory disk. It is constructed with high-performance flash disk controller and good-quality NAND flash memory. This IDE Flash Disk module operates in both 5-Volt and 3.3-Volt power supplies. It comes in capacity of 32MB~ 4GB unformatted disk. Emulating IDE fixed hard disk drives and being fully compatible with ATAPI standard, it is a perfect choice of solid-state mass-storage flash disk for industrial uses or some special applications, or the applications which require high environment tolerance with high data reliability.

It's a very low-power design with flash technology ruggedness, reliability, performance and convenience. Non-recoverable error rate is less than 1 error per 10¹⁵ bit-reads. This IDE Flash Disk has no seek errors. It's solid-state construction requires no preventative maintenance.

Product Features

- **ATA/ IDE interface compliant**
 - Support IDE or ATAPI PIO/ UDMA mode
 - ATA command set compatible
 - Support for 8- or 16-bit host transfers
 - Compatible with host ATA disk I/O BIOS, DOS/Windows file system, utilities, and application softwares

- **Extremely rugged and reliable, shock& vibration resistant**
 - Solid-state reliability
 - 1000G operating / non-operating shock. 15G vibration
 - Built-in 4 symbol ECC

- **High performance**
 - PIO mode 0~ 4 supported
 - UltraDMA mode 0~ 4 supported



- **Disk Capacity**

32MB~ 4 GB supported

- **Single power**

Single +5 Volt or +3.3 Volt power supply.

Very low power consumption with automatic power management.

- **RoHS compliant**

Products Models

Unformatted	Product Model	Cylinder	Head	Sector
FDM601				
32MB	FDM601-032M0xyz	0496	04	32
64MB	FDM601-064M0xyz	0978	04	32
128MB	FDM601-128M0xyz	0978	08	32
256MB	FDM601-256M0xyz	0978	16	32
512MB	FDM601-512M0xyz	0993	16	63
1GB	FDM601-001G0xyz	1985	16	63
2GB	FDM601-002G0xyz	3954	16	63
4GB	FDM601-004G0xyz	7889	16	63
FDM601PRO				
32MB	FDM601-032M1xyz	0496	04	32
64MB	FDM601-064M1xyz	0978	04	32
128MB	FDM601-128M1xyz	0978	08	32
256MB	FDM601-256M1xyz	0978	16	32
512MB	FDM601-512M1xyz	0993	16	63
1GB	FDM601-001G1xyz	1985	16	63
2GB	FDM601-002G1xyz	3954	16	63
4GB	FDM601-004G1xyz	7889	16	63

Note: (1) x is Internal control code, default x = 0.

(2) y is Internal control code, default y = 0.

(3) z defines operation temp.

z = C: Commercial grade;

z = I : Industrial grade(Wide Temp).

Product Specification**Connector type**

40pin IDE

Performance

Burst transfer rate	66.6MB/s
Sustained read	Up to 15 MB/s under ATA Ultra DMA mode 4
Sustained write	Up to 10 MB/s under ATA Ultra DMA mode 4
Sustained read*	Up to 25 MB/s under ATA Ultra DMA mode 4 (FDM601PRO 256MB~ 4GB)*
Sustained write*	Up to 13 MB/s under ATA Ultra DMA mode 4 (FDM601PRO 256MB~ 4GB)*

Command to DREQ	< 4msec
Deep power down to idle	< 4msec
Idle to Read	< 1 μ sec
Idle to Write	< 1 μ sec

Reliability

Error Rate less than 1 bit error in 10^{15} bits read (min)
Internal on-the-fly 4-symbol ECC corrections
Wear-leveling supported
MTBF 2,000,000 hrs
R/W cycle 2,000,000 times

Ruggedness

Shock, operating or non-operating 1,000G, any axis or direction
Vibration, operating or non-operating 15G peak.

Operating Voltage

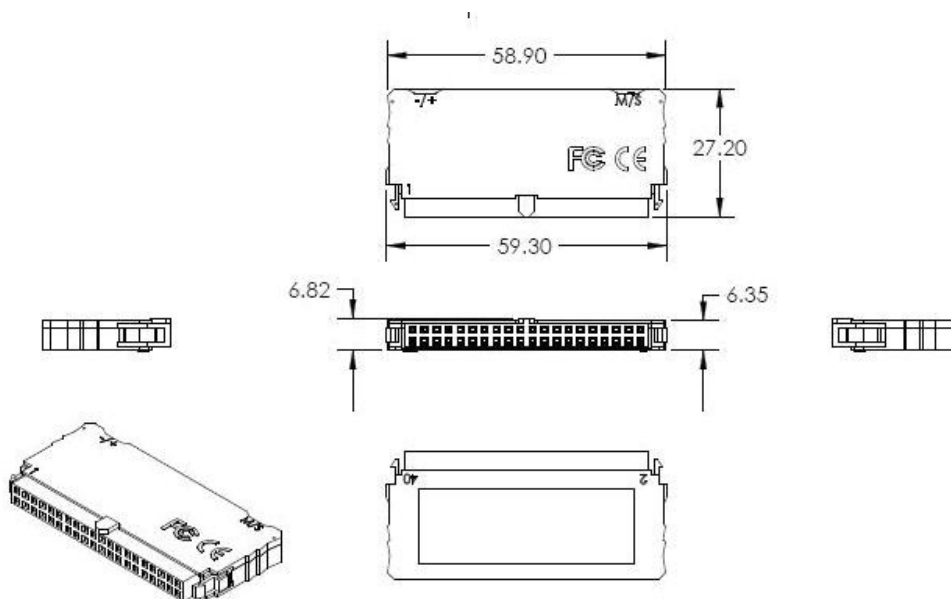
5V +/- 10% or 3.3V +/- 5%

Power consumption :

Read mode	70 mA (typ.)
Write mode	75 mA (typ.)
Sleep mode	1 mA (typ.)

Environment conditions

Operating temperature	0°C to 70°C (Commercial grade) -40°C to 85°C (Industrial grade)
Storage temperature	-20°C to 80°C (Commercial grade) -45°C to 95°C (Industrial grade)
Relative humidity	95%(Max)
Altitude	50,000 ft

Outlines

Length= 59.30mm

Width= 27.20mm

Thickness= 6.82mm

Host IDE connector

Pin No.	Signal name	Pin No.	Signal name
1	RESET	2	Ground
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	Ground	20	(keypin)
21	DMARQ	22	Ground
23	IOWR	24	Ground
25	IORD	26	Ground
27	IORDY	28	CSEL
29	DMACK	30	Ground
31	INTRQ	32	IOCS16; reserved
33	DA1	34	PDIAG
35	DA0	36	DA2
37	CE0	38	CE1
39	DASP	40	Ground

Vcc connector

Pin No.	Signal name
1	Vcc
2	Ground

Signal Descriptions

Signal Name	Dir.	Pin	Description
DASP	I/O	39	This input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
D[15:0]	I/O	18,16,14,12,10,8,6,4,17,15,13,11,9,7,5,3	These lines carry the Data, Commands, and Status information between the host and the controller. All Task File operations occur in byte mode on the lower order bus D00-D07 while all data transfers are 16-bit using D00-D15.
IOWR	I	23	The I/O Write Strobe pulse is used to clock I/O data on the data bus. The clocking will occur on the negative to the positive edge of the signal (trailing edge). (I/O Write / Stop UltraDMA burst)
IORD	I	25	This is an I/O Read strobe generated by the host. (I/O Read / UltraDMA ready / UltraDMA data strobe)
INTRQ	OT	31	This signal is the active high Interrupt Request to the host.
A[2:0]	I	36,33,35	A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host .
CE0,CE1	I	37,38	CE0 is the chip select for the task file registers while CE2 is used to select the Alternate Status Register and the Device Control Register.
CSEL	I	28	This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
IOIS 16	OT	32	This output signal is asserted low when this device is expecting a word data transfer cycle. This signal is used in PIO mode 0,1 and 2 only for ATA-2. This signal must be pulled high by the host.
PDIAG	I/O	34	This input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
IORDY	OT	27	This output signal may be used as IORDY to extended IO cycle time. This signal must be pulled high by the host. (I/O channel ready / UltraDMA ready / UltraDMA data strobe)
DMARQ	O	21	For DMA data transfers, this controller will assert DMARQ when the controller is ready to transfer data to or from the host.
DMACK	I	29	This signal is used by the host in response to DMARQ to initiate DMA transfers.
GND	P	2,22,24,26,30,40,	Ground.
RESET	I	1	This input pin is the active low hardware reset from the host.

Revision History

Revision No.	Histroy	Draft Date	Remark
Preliminary	Preliminary release	Aug. 28, 2006	
V1.0	Initial release	Sep. 1, 2006	
V1.1	FDM601PRO included	Sep. 21, 2006	
V1.2	Update product PN	Oct. 20, 2006	

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